

ISSUE CLASSIFICATION	
Class	Subclass

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

SCANNED

Q. A. L. L.

APPLICATION NO. 09/634068	CONT/PRIOR	CLASS 345 752	SUBCLASS 339 68	ART UNIT 2851 2674 2772	EXAMINER SUAREZ J. CABECA
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FILE

Signal transition and stable regions diagram for positioning a logic analyzer sample

PTO-2040
12/89[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS		CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
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	_____ (Primary Examiner) (Date)		Amount Due	Date Paid
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